

# PHN103T

N-channel enhancement mode field-effect transistor

Rev. 01 — 28 August 2000

Product specification

## 1. Description

N-channel enhancement mode field-effect transistor in a plastic package using TrenchMOS™<sup>1</sup> technology.

Product availability:

PHN103T in SOT96-1 (SO8).

## 2. Features

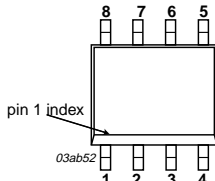
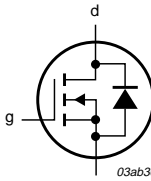
- TrenchMOS™ technology
- Fast switching
- Low on-state resistance
- Logic level compatible
- Surface mount package.

## 3. Applications

- Motor and actuator driver
- Battery management
- High speed, low resistance switch.

## 4. Pinning information

Table 1: Pinning - SOT96-1, simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1,2,3	source (s)		
4	gate (g)		
5,6,7,8	drain (d)		
		<b>SOT96-1 (SO8)</b>	<b>N-channel MOSFET</b>

1. TrenchMOS is a trademark of Royal Philips Electronics.

## 5. Quick reference data

**Table 2: Quick reference data**

Symbol	Parameter	Conditions	Typ	Max	Unit
$V_{DS}$	drain-source voltage (DC)	$T_j = 25$ to $150$ °C	–	30	V
$I_D$	drain current (DC)	$T_{sp} = 25$ °C; $V_{GS} = 4.5$ V	–	8.6	A
$P_{tot}$	total power dissipation	$T_{sp} = 25$ °C	–	6.25	W
$T_j$	junction temperature		–	150	°C
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10$ V; $I_D = 5$ A	20	30	mΩ
		$V_{GS} = 4.5$ V; $I_D = 2.5$ A	30	50	mΩ

## 6. Limiting values

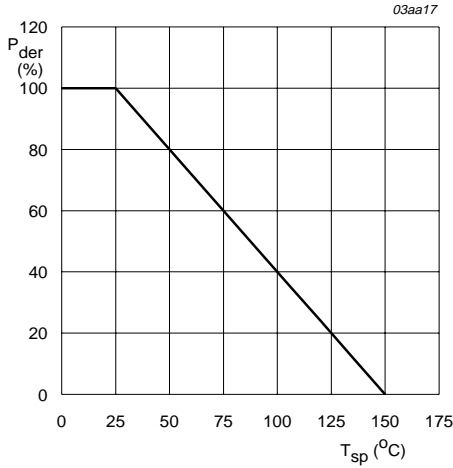
**Table 3: Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage (DC)	$T_j = 25$ to $150$ °C	–	30	V
$V_{DGR}$	drain-gate voltage (DC)	$T_j = 25$ to $150$ °C; $R_{GS} = 20$ kΩ	–	30	V
$V_{GS}$	gate-source voltage (DC)		–	±20	V
$I_D$	drain current (DC)	$T_{sp} = 25$ °C; $V_{GS} = 4.5$ V; Figure 2 and 3	–	8.6	A
		$T_{sp} = 100$ °C; $V_{GS} = 4.5$ V; Figure 2	–	5.4	A
$I_{DM}$	peak drain current	$T_{sp} = 25$ °C; pulsed; $t_p \leq 10$ μs; Figure 3	–	34	A
$P_{tot}$	total power dissipation	$T_{sp} = 25$ °C; Figure 1	–	6.25	W
$T_{stg}$	storage temperature		–65	+150	°C
$T_j$	operating junction temperature		–65	+150	°C

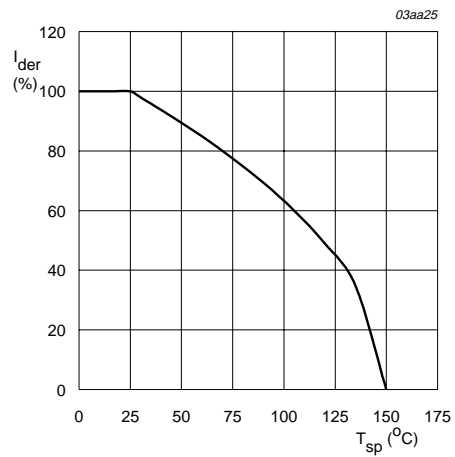
### Source-drain diode

$I_S$	source (diode forward) current (DC)	$T_{sp} = 25$ °C	–	7	A
$I_{SM}$	peak source (diode forward) current	$T_{sp} = 25$ °C; pulsed; $t_p \leq 10$ μs	–	34	A



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

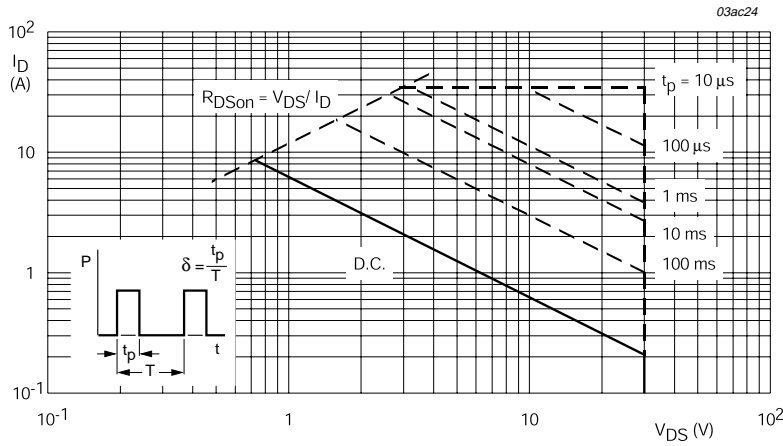
Fig 1. Normalized total power dissipation as a function of solder point temperature.



$$V_{GS} \geq 4.5 \text{ V}$$

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of solder point temperature.



$T_{sp} = 25^{\circ}C$ ;  $I_{DM}$  is single pulse.

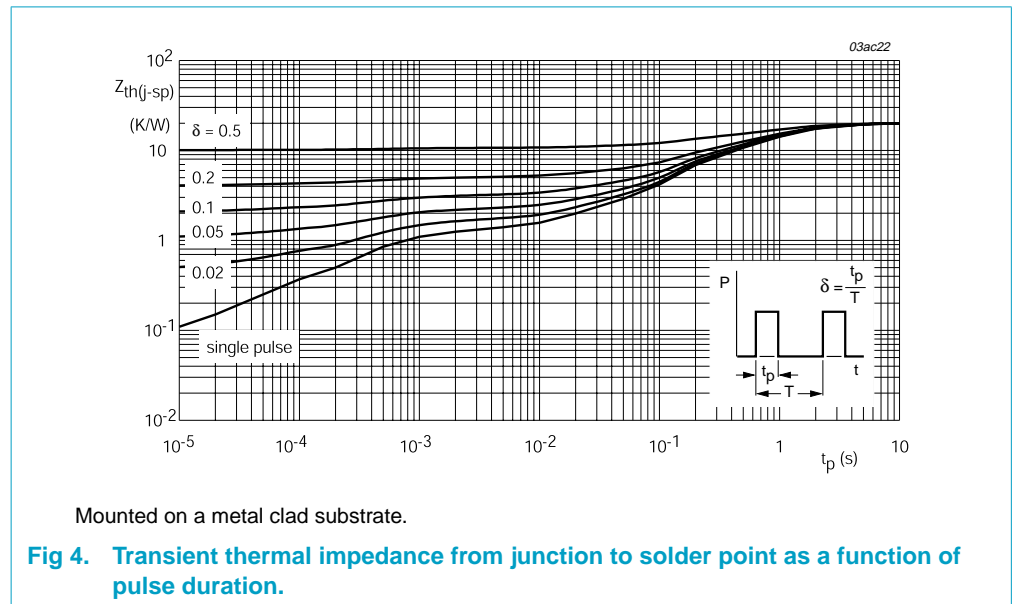
Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

## 7. Thermal characteristics

Table 4: Thermal characteristics

Symbol	Parameter	Conditions	Value	Unit
$R_{th(j-sp)}$	thermal resistance from junction to solder point	mounted on a metal clad substrate; Figure 4	20	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	mounted on a printed circuit board; minimum footprint	150	K/W

### 7.1 Transient thermal impedance



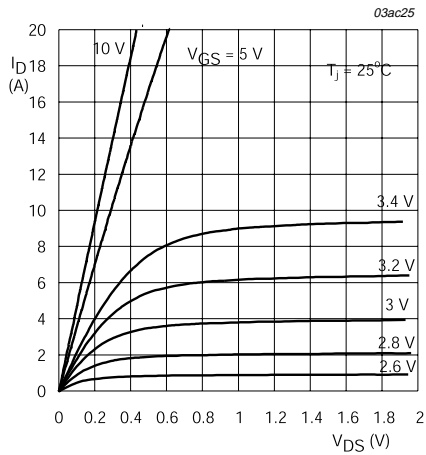
## 8. Characteristics

**Table 5: Characteristics**
*T<sub>j</sub> = 25 °C unless otherwise specified*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
V <sub>(BR)DSS</sub>	drain-source breakdown voltage	I <sub>D</sub> = 10 μA; V <sub>GS</sub> = 0 V T <sub>j</sub> = 25 °C	30	43	–	V
		T <sub>j</sub> = –55 °C	27	–	–	V
V <sub>GS(th)</sub>	gate-source threshold voltage	I <sub>D</sub> = 1 mA; V <sub>DS</sub> = V <sub>GS</sub> ; Figure 9				
		T <sub>j</sub> = 25 °C	1	2	2.8	V
		T <sub>j</sub> = 150 °C	0.6	–	–	V
		T <sub>j</sub> = –55 °C	–	–	3.5	V
I <sub>DSS</sub>	drain-source leakage current	V <sub>DS</sub> = 24 V; V <sub>GS</sub> = 0 V T <sub>j</sub> = 25 °C	–	10	100	nA
		T <sub>j</sub> = 150 °C	–	–	10	μA
I <sub>GSS</sub>	gate-source leakage current	V <sub>GS</sub> = ±20 V; V <sub>DS</sub> = 0 V	–	10	100	nA
R <sub>DS(on)</sub>	drain-source on-state resistance	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 5 A; Figure 7 and 8				
		T <sub>j</sub> = 25 °C	–	20	30	mΩ
		V <sub>GS</sub> = 5 V; I <sub>D</sub> = 2.5 A; Figure 7 and 8				
		T <sub>j</sub> = 25 °C	–	30	50	mΩ
		T <sub>j</sub> = 150 °C	–	–	85	mΩ
<b>Dynamic characteristics</b>						
g <sub>fs</sub>	forward transconductance	V <sub>DS</sub> = 5 V; I <sub>D</sub> = 5.5 A; Figure 11	–	12	–	S
Q <sub>g(tot)</sub>	total gate charge	I <sub>D</sub> = 5 A; V <sub>DS</sub> = 15 V;	–	24	40	nC
Q <sub>gs</sub>	gate-source charge	V <sub>GS</sub> = 10 V; Figure 14	–	3.3	–	nC
Q <sub>gd</sub>	gate-drain (Miller) charge		–	7.4	–	nC
C <sub>iss</sub>	input capacitance	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 24 V;	–	770	–	pF
C <sub>oss</sub>	output capacitance	f = 1 MHz; Figure 12	–	265	–	pF
C <sub>rss</sub>	reverse transfer capacitance		–	180	–	pF
t <sub>d(on)</sub>	turn-on delay time	V <sub>DD</sub> = 15 V; R <sub>D</sub> = 15 Ω;	–	8	–	ns
t <sub>r</sub>	turn-on rise time	V <sub>GS</sub> = 10 V; R <sub>G</sub> = 6 Ω	–	10	–	ns
t <sub>on</sub>	turn-on time		–	18	35	ns
t <sub>d(off)</sub>	turn-off delay time		–	24	–	ns
t <sub>f</sub>	turn-off fall time		–	20	–	ns
t <sub>off</sub>	turn-off time		–	44	150	ns

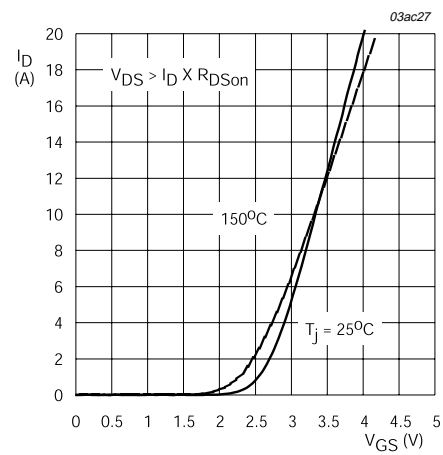
**Table 5: Characteristics...continued**  
 $T_j = 25\text{ }^\circ\text{C}$  unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Source-drain diode</b>						
$V_{SD}$	source-drain (diode forward) voltage	$I_S = 1.25\text{ A}$ ; $V_{GS} = 0\text{ V}$ ; Figure 13	–	0.73	1.0	V
$t_{rr}$	reverse recovery time	$I_S = 1.25\text{ A}$ ; $di_S/dt = -100\text{ A}/\mu\text{s}$ ;	–	120	–	ns
$Q_r$	recovered charge	$V_{GS} = 0\text{ V}$ ; $V_{DS} = 25\text{ V}$	–	150	–	nC



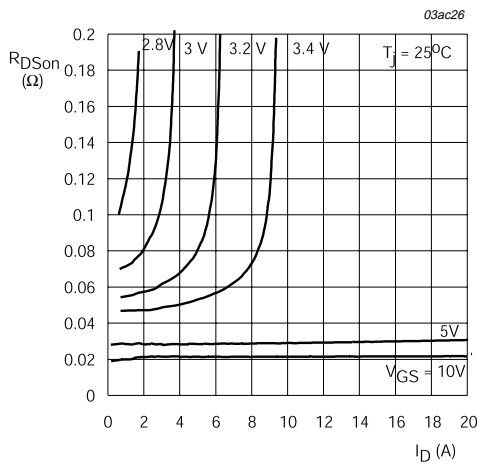
$T_j = 25\text{ }^\circ\text{C}$

**Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.**



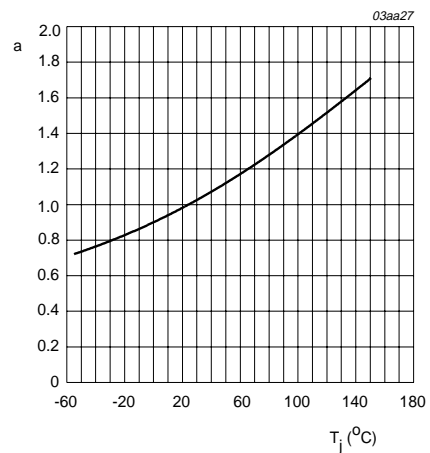
$T_j = 25\text{ }^\circ\text{C}$  and  $150\text{ }^\circ\text{C}$ ;  $V_{DS} > I_D \times R_{DSon}$

**Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.**



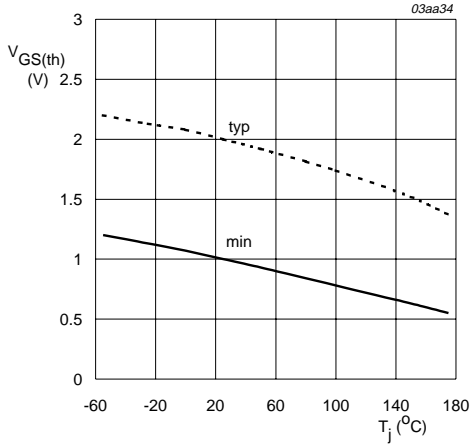
$T_j = 25\text{ }^\circ\text{C}$

**Fig 7. Drain-source on-state resistance as a function of drain current; typical values.**



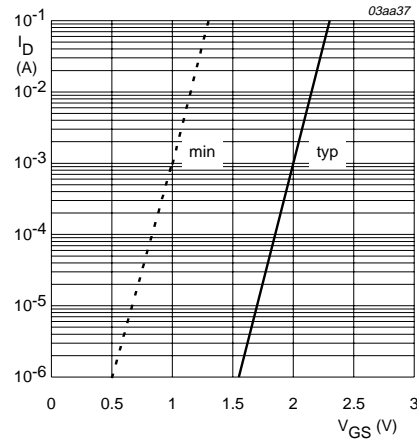
$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$

**Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.**



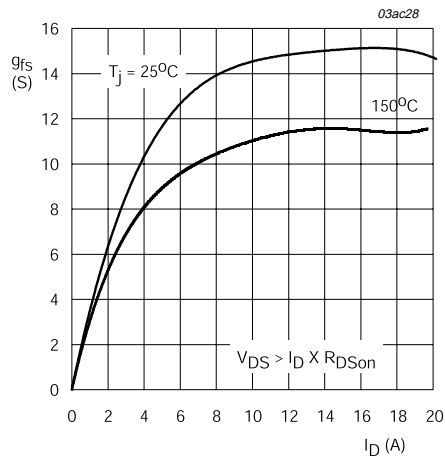
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

**Fig 9. Gate-source threshold voltage as a function of junction temperature.**



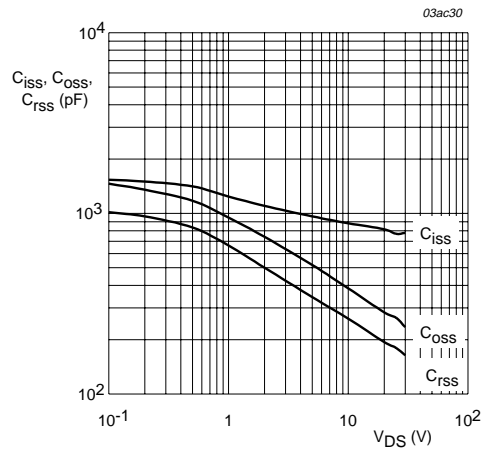
$T_j = 25 \text{ }^\circ\text{C}; V_{DS} = 5 \text{ V}$

**Fig 10. Sub-threshold drain current as a function of gate-source voltage.**



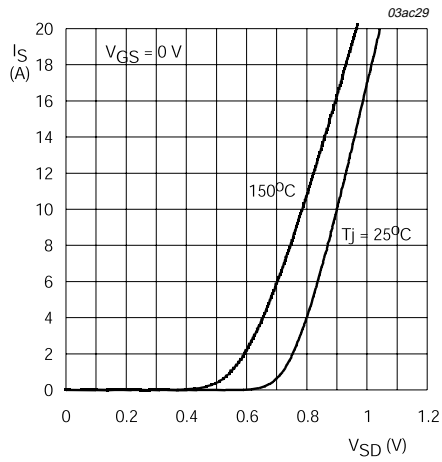
$T_j = 25 \text{ }^\circ\text{C}$  and  $150 \text{ }^\circ\text{C}; V_{DS} > I_D \times R_{DS(on)}$

**Fig 11. Forward transconductance as a function of drain current; typical values.**



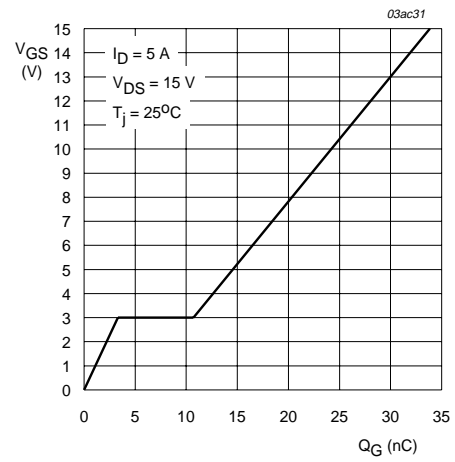
$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

**Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.**



$T_j = 25^\circ\text{C}$  and  $150^\circ\text{C}$ ;  $V_{GS} = 0\text{ V}$

**Fig 13. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.**



$I_D = 5\text{ A}$ ;  $V_{DS} = 15\text{ V}$

**Fig 14. Gate-source voltage as a function of gate charge; typical values.**



9. Package outline

SO8: plastic small outline package; 8 leads; body width 3.9 mm

SOT96-1

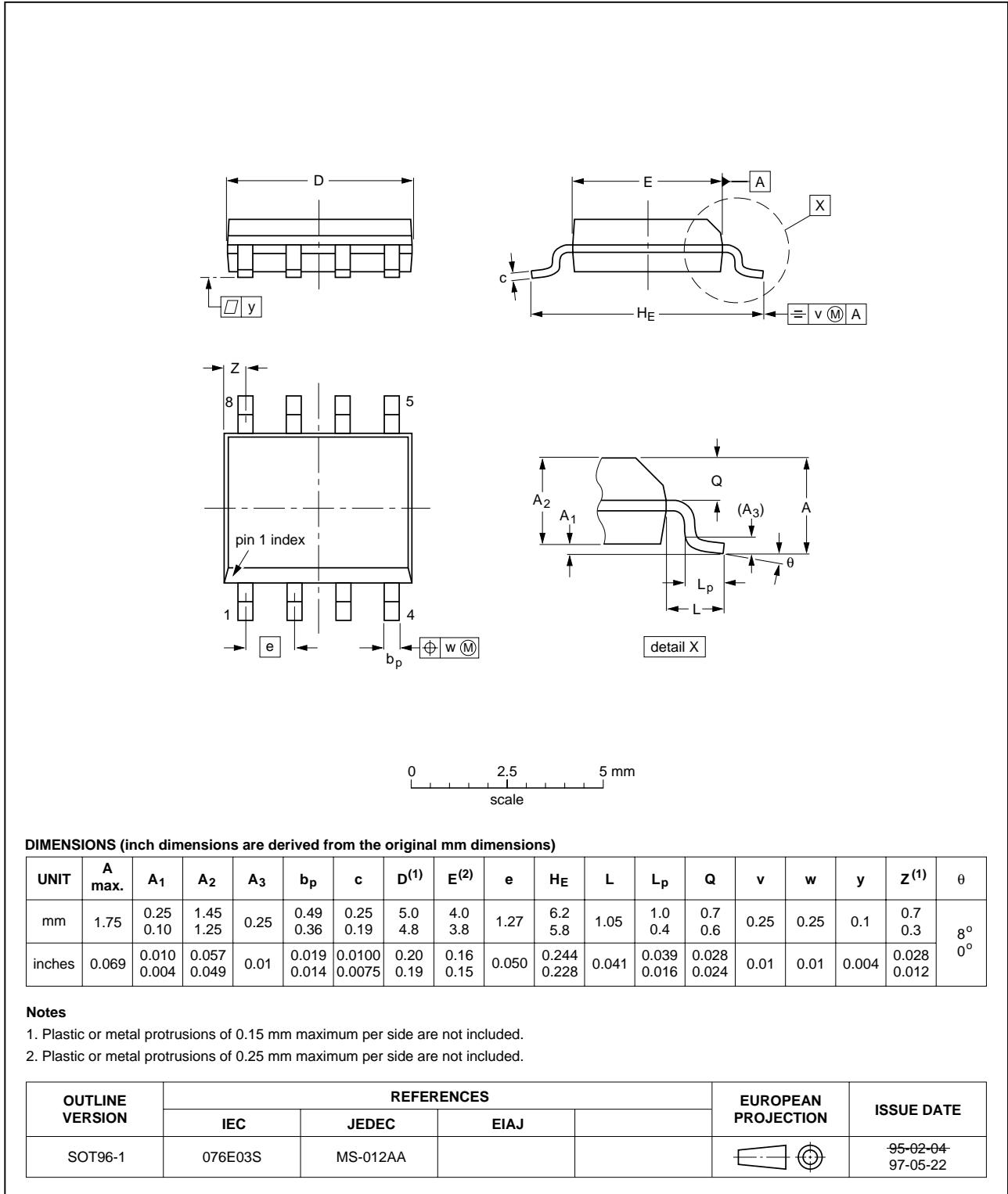


Fig 15. SOT96-1 (SO8).

## 10. Revision history

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Table 6: Revision history

Rev	Date	CPCN	Description
01	20000828	HZG336	<b>Product specification; initial version.</b> Converted from VDMOS (Nijmegen) to TrenchMOS™ technology (Hazel Grove).

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## 11. Data sheet status

Datasheet status	Product status	Definition <sup>[1]</sup>
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

[1] Please consult the most recently issued data sheet before initiating or completing a design.

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**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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**Denmark:** Tel. +45 3 288 2636, Fax. +45 3 157 0044

**Finland:** Tel. +358 961 5800, Fax. +358 96 158 0920

**France:** Tel. +33 14 099 6161, Fax. +33 14 099 6427

**Germany:** Tel. +49 40 23 5360, Fax. +49 402 353 6300

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**India:** Tel. +91 22 493 8541, Fax. +91 22 493 8722

**Indonesia:** see Singapore

**Ireland:** Tel. +353 17 64 0000, Fax. +353 17 64 0200

**Israel:** Tel. +972 36 45 0444, Fax. +972 36 49 1007

**Italy:** Tel. +39 039 203 6838, Fax. +39 039 203 6800

**Japan:** Tel. +81 33 740 5130, Fax. +81 3 3740 5057

**Korea:** Tel. +82 27 09 1412, Fax. +82 27 09 1415

**Malaysia:** Tel. +60 37 50 5214, Fax. +60 37 57 4880

**Mexico:** Tel. +9-5 800 234 7381

**Middle East:** see Italy

**For all other countries apply to:** Philips Semiconductors,  
Marketing Communications,  
Building BE, P.O. Box 218, 5600 MD EINDHOVEN,  
The Netherlands, Fax. +31 40 272 4825

**Netherlands:** Tel. +31 40 278 2785, Fax. +31 40 278 8399

**New Zealand:** Tel. +64 98 49 4160, Fax. +64 98 49 7811

**Norway:** Tel. +47 22 74 8000, Fax. +47 22 74 8341

**Philippines:** Tel. +63 28 16 6380, Fax. +63 28 17 3474

**Poland:** Tel. +48 22 5710 000, Fax. +48 22 5710 001

**Portugal:** see Spain

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**Russia:** Tel. +7 095 755 6918, Fax. +7 095 755 6919

**Singapore:** Tel. +65 350 2538, Fax. +65 251 6500

**Slovakia:** see Austria

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**South Africa:** Tel. +27 11 471 5401, Fax. +27 11 471 5398

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**Ukraine:** Tel. +380 44 264 2776, Fax. +380 44 268 0461

**United Kingdom:** Tel. +44 208 730 5000, Fax. +44 208 754 8421

**United States:** Tel. +1 800 234 7381

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